What is claimed is:

1. Apparatus comprising:

a semiconductor body having on a surface thereof at least one lower antifuse and at least one upper antifuse in vertically stacked relation with both such antifuses sharing a common intermediate electrode therebetween;

the lower antifuse having a lower counter electrode and a lower fusible insulator portion defining a lower fuse element of an initial high electrical resistance state interconnecting the lower counter electrode with the common intermediate electrode; and

the upper antifuse having an upper counter electrode and an upper fusible insulator portion defining an upper fuse element of an initial high electrical resistance state interconnecting the upper counter electrode with the common intermediate electrode;

the upper and lower antifuses being arranged to permit their respective selective energizing for corresponding separate or simultaneous activation to a final low electrical resistance state.

2. The apparatus of claim 1 wherein at least one of the antifuses is provided redundantly with at least one additional antifuse in closely laterally adjacent arrangement thereto and having an additional counter electrode and an additional fusible insulator portion defining an additional fuse element of an initial high electrical resistance state interconnecting the additional counter electrode with the common intermediate

electrode.

3. The apparatus of claim 1 wherein the lower antifuse is provided redundantly with at least one additional lower antifuse in closely laterally adjacent arrangement thereto and connected in parallel therewith and having an additional lower counter electrode and an additional lower fusible insulator portion defining an additional lower fuse element of an initial high electrical resistance state interconnecting the additional lower counter electrode with the common intermediate electrode.

4. The apparatus of claim 3 wherein the upper antifuse is provided redundantly with at least one additional upper antifuse in closely laterally adjacent arrangement thereto and connected in parallel therewith and having an additional upper counter electrode and an additional upper fusible insulator portion defining an additional upper fuse element of an initial high electrical resistance state interconnecting the additional upper counter electrode with the common intermediate electrode.

5. The apparatus of claim 1 wherein the upper antifuse is provided redundantly with at least one additional upper antifuse in closely laterally adjacent arrangement thereto and connected in parallel therewith and having an additional upper counter electrode and an additional upper fusible insulator portion defining an additional upper fuse element of an initial high electrical resistance state interconnecting the additional upper counter electrode with the common intermediate electrode.

6. The apparatus of claim 1 wherein the counter electrode of at least one of the antifuses is interconnected by the

corresponding fuse element to the common intermediate electrode through at least one electrode extension portion interposed between said fuse element and the common intermediate electrode.

7. The apparatus of claim 1 wherein the counter electrode of at least one of the antifuses is interconnected by the corresponding fuse element to the common intermediate electrode through at least one electrode extension portion interposed between said fuse element and the corresponding counter electrode.

8. The apparatus of claim 1 wherein the lower antifuse is in the form of a gate oxide antifuse having a source region and a drain region correspondingly closely laterally adjacent the lower fusible insulator portion defining the lower fuse element, a gate oxide electrode in contact with the lower fuse element and forming the lower counter electrode, a source conductive extension portion interposed between the source region and the common intermediate electrode, the source conductive extension portion and source region together defining a source electrode extension portion, and a drain conductive extension portion interposed between the drain region and the common intermediate electrode, the drain conductive extension portion and drain region together defining a drain electrode extension portion, for interconnecting the gate electrode by the lower fuse element with the common intermediate electrode through the source electrode extension portion and through the drain electrode extension portion.

9. The apparatus of claim 1 wherein the upper antifuse is

in the form of a contact antifuse having an electrode extension portion defining a conductive contact interposed between the upper counter electrode and the upper fusible insulator portion defining the upper fuse element and interconnecting the upper counter electrode with the upper fuse element, the upper fuse element also being interconnected with the common intermediate electrode.

10. The apparatus of claim 9 wherein the upper fuse element is directly interconnected with the common intermediate electrode.

11. The apparatus of claim 1 wherein the lower antifuse is in the form of a contact antifuse having an electrode extension portion defining a conductive contact interposed between the common intermediate electrode and the lower fusible insulator portion defining the lower fuse element and interconnecting the common intermediate electrode with the lower fuse element, the lower fuse element also being interconnected with the lower counter electrode.

12. The apparatus of claim 11 wherein the lower fuse element is directly interconnected with the lower counter electrode.

13. The apparatus of claim 11 wherein the lower counter electrode is in the form of a diffusion region in contact with the lower fuse element.

14. The apparatus of claim 11 wherein the upper antifuse is in the form of a contact antifuse having an electrode extension portion defining a conductive contact interposed between the

upper counter electrode and the upper fusible insulator portion defining the upper fuse element and interconnecting the upper counter electrode with the upper fuse element, the upper fuse element also being interconnected with the common intermediate electrode.

15. The apparatus of claim 14 wherein the upper fuse element is directly interconnected with the common intermediate electrode.

16. The apparatus of claim 1 further comprising energizable fuse activation circuit means defining a lower fuse activation circuit for applying and controlling a selective blow voltage across the lower counter electrode and common intermediate electrode at the lower fuse element for fusibly blowing the lower antifuse to a final low electrical resistance state to interconnect electrically conductively the lower counter electrode and the common intermediate electrode thereat, and further defining an upper fuse activation circuit for applying and controlling a selective blow voltage across the upper counter electrode and common intermediate electrode at the upper fuse element for fusibly blowing the upper antifuse to a final low electrical resistance state to interconnect electrically conductively the upper counter electrode and the common intermediate electrode thereat.

17. The apparatus of claim 16 further comprising unblown or blown fuse activation state sensing and indicating circuit means defining a lower fuse state sensing and indicating circuit for sensing and indicating the unblown or blown fuse activation state

of the lower antifuse, and further defining an upper fuse state sensing and indicating circuit for sensing and indicating the unblown or blown fuse activation state of the upper antifuse.

18. The apparatus of claim 16 wherein the fuse activation circuit means are arranged for independently applying and controlling a selective blow voltage for fusibly blowing the lower antifuse, and for independently applying and controlling a selective blow voltage for fusibly blowing the upper antifuse, to permit their respective selective energizing for corresponding separate fuse activation.

19. The apparatus of claim 16 wherein the fuse activation circuit means are arranged for simultaneously applying and controlling a selective blow voltage for fusibly blowing both the lower antifuse and upper antifuse, to permit their selective energizing for simultaneous fuse activation.

20. The apparatus of claim 19 wherein the lower antifuse and upper antifuse are connected in parallel in the fuse activation circuit.

21. A semiconductor device comprising:

a wafer having on a surface thereof an arrangement of at least one lower antifuse and at least one upper antifuse in vertically stacked relation and both such antifuses sharing a common intermediate electrode therebetween;

the lower antifuse having a lower counter electrode and a lower fusible insulator portion defining a lower fuse element of an initial high electrical resistance state interconnecting the lower counter electrode with the common intermediate

electrode; and

the upper antifuse having an upper counter electrode and an upper fusible insulator portion defining an upper fuse element of an initial high electrical resistance state interconnecting the upper counter electrode with the common intermediate electrode;

the upper and lower antifuses being arranged to permit their respective selective energizing for corresponding separate or simultaneous activation to a final low electrical resistance state;

wherein at least one of the antifuses is provided redundantly with at least one additional antifuse in closely laterally adjacent arrangement thereto and having an additional counter electrode and an additional fusible insulator portion defining an additional fuse element of an initial high electrical resistance state interconnecting the additional counter electrode with the common intermediate electrode; and

wherein the counter electrode of at least one of the antifuses is interconnected by the corresponding fuse element to the common intermediate electrode through at least one electrode extension portion interposed between said fuse element and the common intermediate electrode.

22. A semiconductor device comprising:

a wafer having on a surface thereof an arrangement of at least one lower antifuse and at least one upper antifuse in vertically stacked relation and both such antifuses sharing a common intermediate electrode therebetween;

the lower antifuse having a lower counter electrode and a lower fusible insulator portion defining a lower fuse element of an initial high electrical resistance state interconnecting the lower counter electrode with the common intermediate electrode; and

the upper antifuse having an upper counter electrode and an upper fusible insulator portion defining an upper fuse element of an initial high electrical resistance state interconnecting the upper counter electrode with the common intermediate electrode;

the upper and lower antifuses being arranged to permit their respective selective energizing for corresponding separate or simultaneous activation to a final low electrical resistance state;

wherein at least one of the antifuses is provided redundantly with at least one additional antifuse in closely laterally adjacent arrangement thereto and having an additional counter electrode and an additional fusible insulator portion defining an additional fuse element of an initial high electrical resistance state interconnecting the additional counter electrode with the common intermediate electrode; and

wherein the counter electrode of at least one of the antifuses is interconnected by the corresponding fuse element to the common intermediate electrode through at least one electrode extension portion interposed between said fuse element and the corresponding counter electrode.

23. A semiconductor device comprising:

a wafer having on a surface thereof an arrangement of at least one lower antifuse and at least one upper antifuse in vertically stacked relation and both such antifuses sharing a common intermediate electrode therebetween;

the lower antifuse having a lower counter electrode and a lower fusible insulator portion defining a lower fuse element of an initial high electrical resistance state interconnecting the lower counter electrode with the common intermediate electrode; and

the upper antifuse having an upper counter electrode and an upper fusible insulator portion defining an upper fuse element of an initial high electrical resistance state interconnecting the upper counter electrode with the common intermediate electrode;

the upper and lower antifuses being arranged to permit their respective selective energizing for corresponding separate or simultaneous activation to a final low electrical resistance state;

wherein the lower antifuse is provided redundantly with at least one additional lower antifuse in closely laterally adjacent arrangement thereto and connected in parallel therewith and having an additional lower counter electrode and an additional lower fusible insulator portion defining an additional lower fuse element of an initial high electrical resistance state interconnecting the additional lower counter electrode with the common intermediate electrode;

wherein the upper antifuse is provided redundantly with

at least one additional upper antifuse in closely laterally adjacent arrangement thereto and connected in parallel therewith and having an additional upper counter electrode and an additional upper fusible insulator portion defining an additional upper fuse element of an initial high electrical resistance state interconnecting the additional upper counter electrode with the common intermediate electrode; and

wherein the counter electrode of at least one of the antifuses is interconnected by the corresponding fuse element to the common intermediate electrode through at least one electrode extension portion interposed between said fuse element and the common intermediate electrode.

24. A semiconductor device comprising:

a wafer having on a surface thereof an arrangement of at least one lower antifuse and at least one upper antifuse in vertically stacked relation and both such antifuses sharing a common intermediate electrode therebetween;

the lower antifuse having a lower counter electrode and a lower fusible insulator portion defining a lower fuse element of an initial high electrical resistance state interconnecting the lower counter electrode with the common intermediate electrode; and

the upper antifuse having an upper counter electrode and an upper fusible insulator portion defining an upper fuse element of an initial high electrical resistance state interconnecting the upper counter electrode with the common intermediate electrode;

the upper and lower antifuses being arranged to permit their respective selective energizing for corresponding separate or simultaneous activation to a final low electrical resistance state;

wherein the lower antifuse is provided redundantly with at least one additional lower antifuse in closely laterally adjacent arrangement thereto and connected in parallel therewith and having an additional lower counter electrode and an additional lower fusible insulator portion defining an additional lower fuse element of an initial high electrical resistance state interconnecting the additional lower counter electrode with the common intermediate electrode;

wherein the upper antifuse is provided redundantly with at least one additional upper antifuse in closely laterally adjacent arrangement thereto and connected in parallel therewith and having an additional upper counter electrode and an additional upper fusible insulator portion defining an additional upper fuse element of an initial high electrical resistance state interconnecting the additional upper counter electrode with the common intermediate electrode; and

wherein the counter electrode of at least one of the antifuses is interconnected by the corresponding fuse element to the common intermediate electrode through at least one electrode extension portion interposed between said fuse element and the corresponding counter electrode.

25. A semiconductor device comprising:

a wafer having on a surface thereof an arrangement of a

plurality of lower antifuses and a plurality of upper antifuses in vertically stacked relation and sharing a common intermediate electrode therebetween;

the plurality of lower antifuses being in closely laterally adjacent side by side arrangement, each lower antifuse having a lower counter electrode and a lower fusible insulator portion defining a lower fuse element of an initial high electrical resistance state interconnecting the lower counter electrode with the common intermediate electrode, the plurality of lower antifuses being arranged to form a lower bank of antifuses along the common intermediate electrode; and

the plurality of upper antifuses being in closely laterally adjacent side by side arrangement, each upper antifuse having an upper counter electrode and an upper fusible insulator portion defining an upper fuse element of an initial high electrical resistance state interconnecting the upper counter electrode with the common intermediate electrode, the plurality of upper antifuses being arranged to form a corresponding upper bank of antifuses along the common intermediate electrode;

the upper and lower antifuses being arranged to permit their respective selective energizing for corresponding separate or simultaneous activation to a final low electrical resistance state.

26. The semiconductor device of claim 25 wherein at least two of the antifuses are connected in parallel with each other.

27. The semiconductor device of claim 25 wherein at least two of the lower antifuses are connected in parallel with each

other and at least two of the upper antifuses are connected in parallel with each other.